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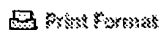
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4 A 68-ns 4-Mbit CMOS EPROM with high-noise-immunity design

Imamiya, K.; Miyamoto, J.; Atsumi, S.; Ohtsuka, N.; Muroya, Y.; Sako, T.;

Higashino, M.; Iyama, Y.; Mori, S.; Ohshima, Y.; Araki, H.; Kaneko, Y.; Narita, K. Arai, N.; Yoshikawa, K.; Tanaka, S.;

Solid-State Circuits, IEEE Journal of, Volume: 25, Issue: 1, Feb. 1990

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5 Design and analysis of a high-speed sense amplifier for single-transist nonvolatile memory cells

Amin, A.A.M.;

Circuits, Devices and Systems, IEE Proceedings G, Volume: 140, Issue: 2, Apr

1993

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6 Development of a variable rate syndrome sequential decoder based on stack algorithm

Ohashi, M.; Yasuda, Y.; Hirata, Y.;

Global Telecommunications Conference, 1988, and Exhibition. 'Communications of the Information Age.' Conference Record, GLOBECOM '88., IEEE , 28 Nov.-1 Dec. 1988

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Wen Xu; Marke, M.;

Personal, Indoor and Mobile Radio Communications, 2001 12th IEEE International Symposium on , Volume: 1 , 30 Sept.-3 Oct. 2001

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